

## C3 DRK

### Digital Radio Kit

Colorado Electronic Product Design Rev 1.1 March 1, 2010

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The Digital Radio Kit (DRK) is intended to aid in the development and test of algorithms and signal processing applications including:

- Digital radio, modulator/demodulator development
- Software defined radio
- High speed data acquisition and signal processing
- Audio data acquisition and signal processing



### Description

The system combines a PCI card, an FPGA signal processing card, and an up/down converting digital radio card. The mixers can be bypassed for direct sampling operation. All three cards have connectors allowing them to stack, forming a digital radio system. The kit will operate in standalone mode using a 12V power supply or the PCI card can be attached to a computer.

The standard configuration for the digital radio card is the 75MHz to 150MHz band. The digital radio card is capable of transmitting and receiving RF signals. Filters, Low Noise Amplifiers, and mixers are socket-ed to simplify frequency changes. The card includes National Semiconductor LMX2313USLD, a frequency synthesizer LO and mixers for up and down conversion for transmitting and receiving. The card utilizes the TI ADS5440, a 13-bit, 210 million samples per second (MSPS) analog-to-digital converter (ADC), the TI DAC5674, a 14-bit, 400 MSPS digital-to-analog converter (DAC) and a TI PCM3500E, an audio codec. The audio codec has line in and line out jacks.

The acquired signals are sampled and then digitally processed by the customizable Altera Cyclone III® EP3C16F484C8N, 180,000 gate FPGA card. Users may customize the FPGA to implement their own algorithms. The FPGA card comes with a JTAG programming connector and a configuration PROM, Altera EPCS16SI16N, to retain the FPGA settings.

The PCI card provides interfaces for the FPGA card to a computer PCI bus, RS232, user push buttons, and LED indicators. 2 computer PCI slots are required if the DRK is used in a PC. The PCI interface utilizes a PLX PCI9030 chip to avoid using any resources in the PCI core, to maximize the space in the FPGA. The PLX is PCI v2.2 compliant and operates at a bus speed of 33MHz and has a data width of 32 bits. The PLX example code was not created to do bursting

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or DMA. A Windows® XP driver for the PCI chip and an example windows application is provided with the kit.

The digital radio card is set up as half duplex up and down conversion with a 10.7MHz IF. The local oscillator is created by the synthesizer controlled by the FPGA. The up/down conversion may be bypassed if the user wants to sample the RF. The digital radio card can directly connect to an antenna using a SMA connection. The radio board is configured for the United States FM radio band, 88.1MHz to 107.9 MHz in 200 KHz steps.

A Digital Radio reference FPGA design example, schematics and VHDL code are provided with the kit. The reference design includes a FM band broadcast transceiver, synthesizer control, demodulator, modulator, RF AD interface, RF DA interface, audio codec interface, RS232 driver, and up/down tuning capability.

If the digital radio card is removed, the remaining two boards form a FPGA/PCI Development Board which provides 86 I/O pins.

## Specifications

Parameter	Minimum	Typical	Maximum	Units
Operating Temperature		25		°C
Input Voltage	9	12	15	VDC
Stand Alone Current Draw		400		mA
Oscillator		133		MHz <sup>1</sup>
PCI Bus Speed		33		MHz

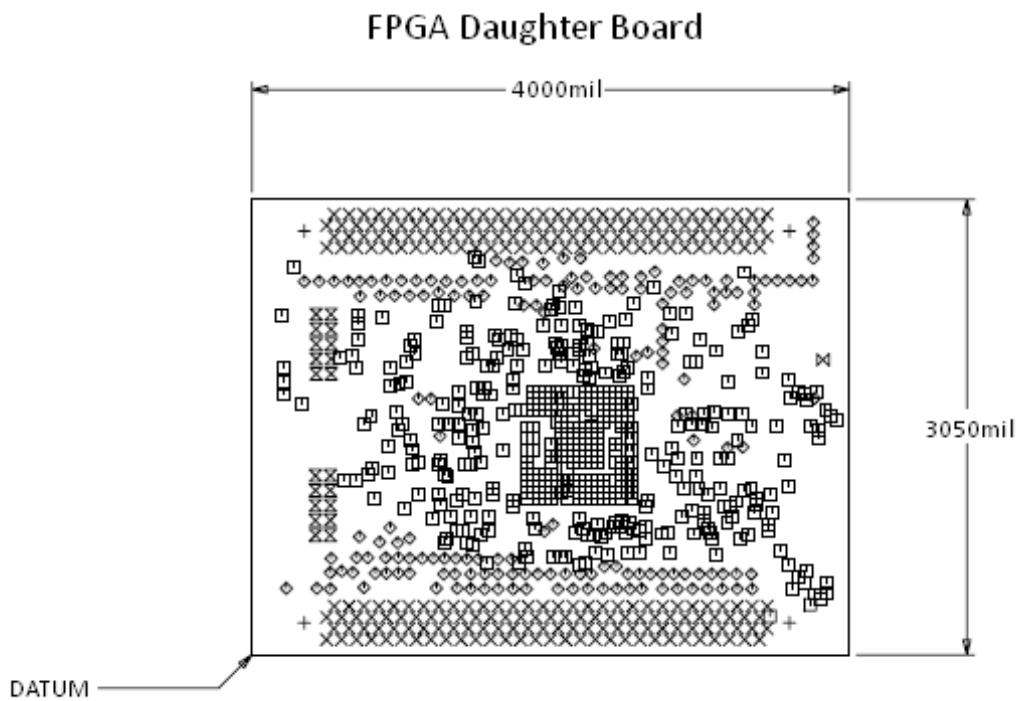
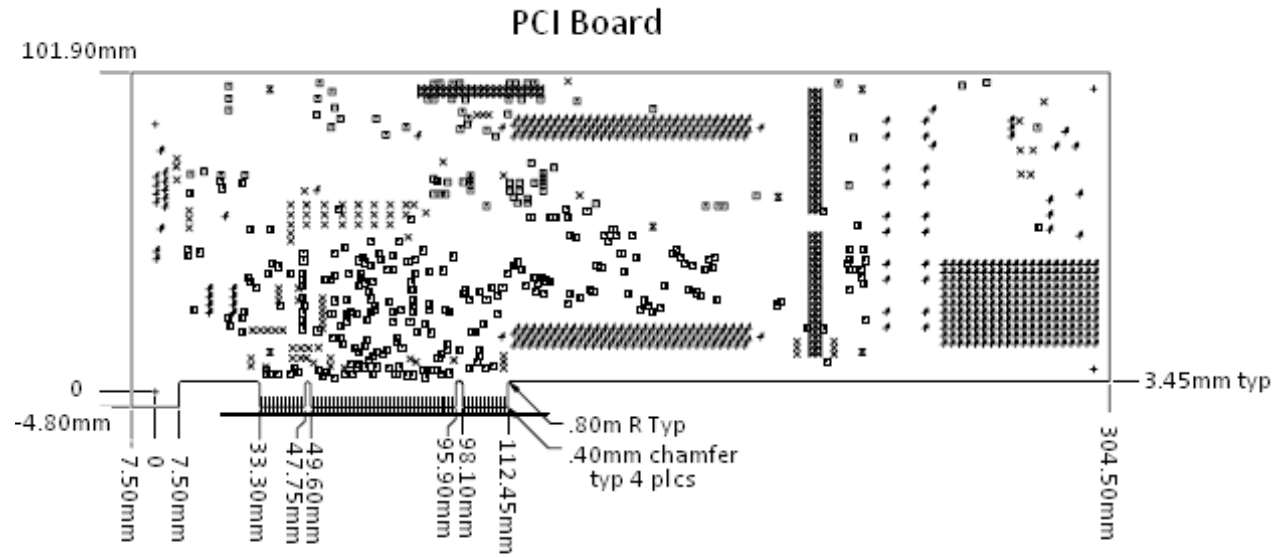
<sup>1</sup> ±50ppm

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## Mechanical Specifications

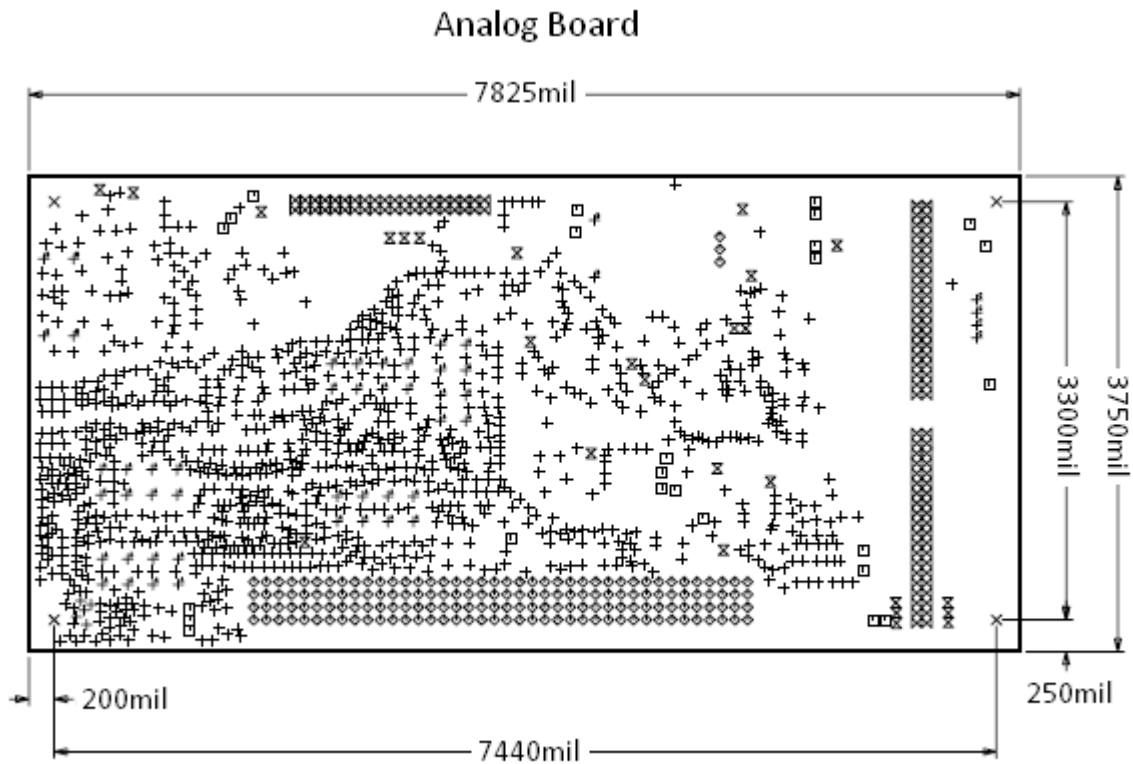


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The PCI Development Kit ships with:

- Bill of Materials
  - PCI Board Bill of Materials
  - Altera Cyclone III<sup>®</sup> daughter board
  - Analog Board
- Data Sheets
  - Altera Cyclone III<sup>®</sup> EP3C16F484C8N
  - Altera EEPROM EPCS16SI16N
- Windows<sup>®</sup> XP PCI Driver
- Schematics
  - PCI Board
  - Altera Cyclone III daughter board
  - Analog Board
- VHDL Examples
  - DRK example code
- User Manual

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## C3 DRK

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- 12 volt wall mount power supply

## Diagrams

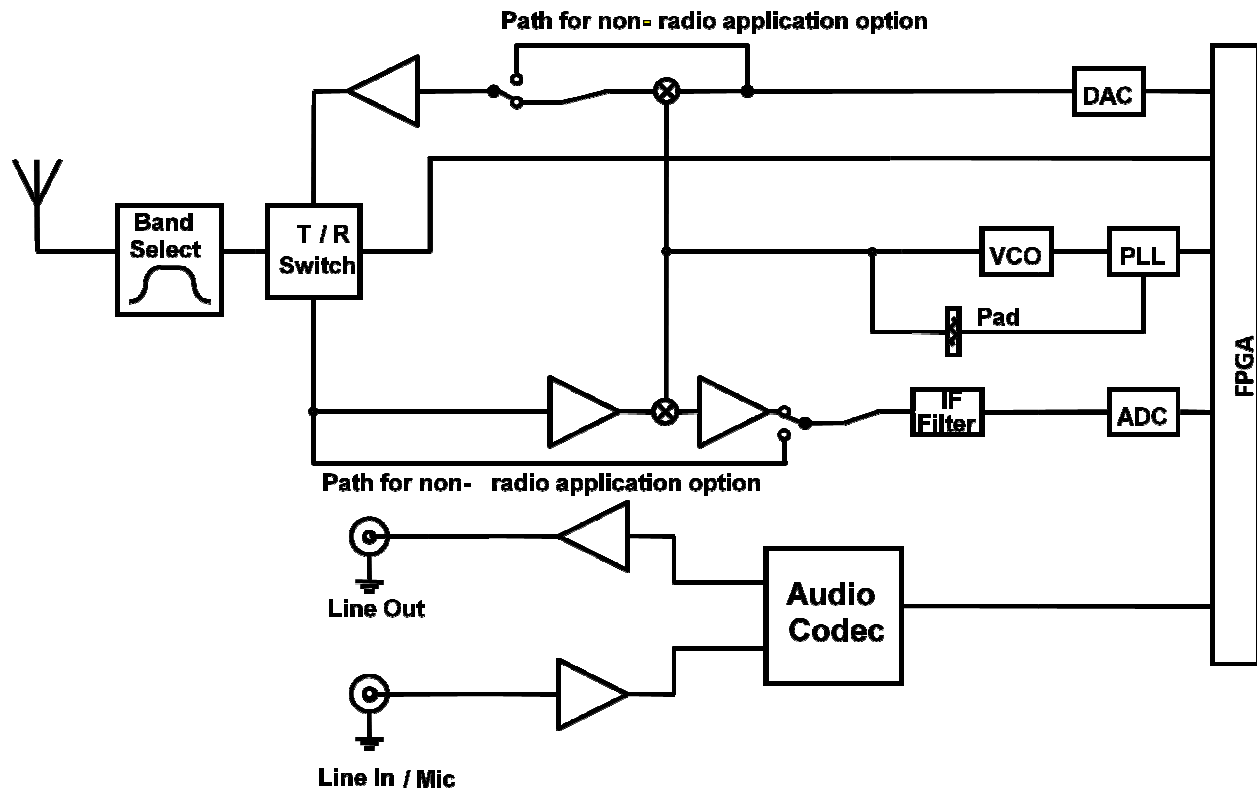


Figure 1 - Block Diagram of the Analog Board

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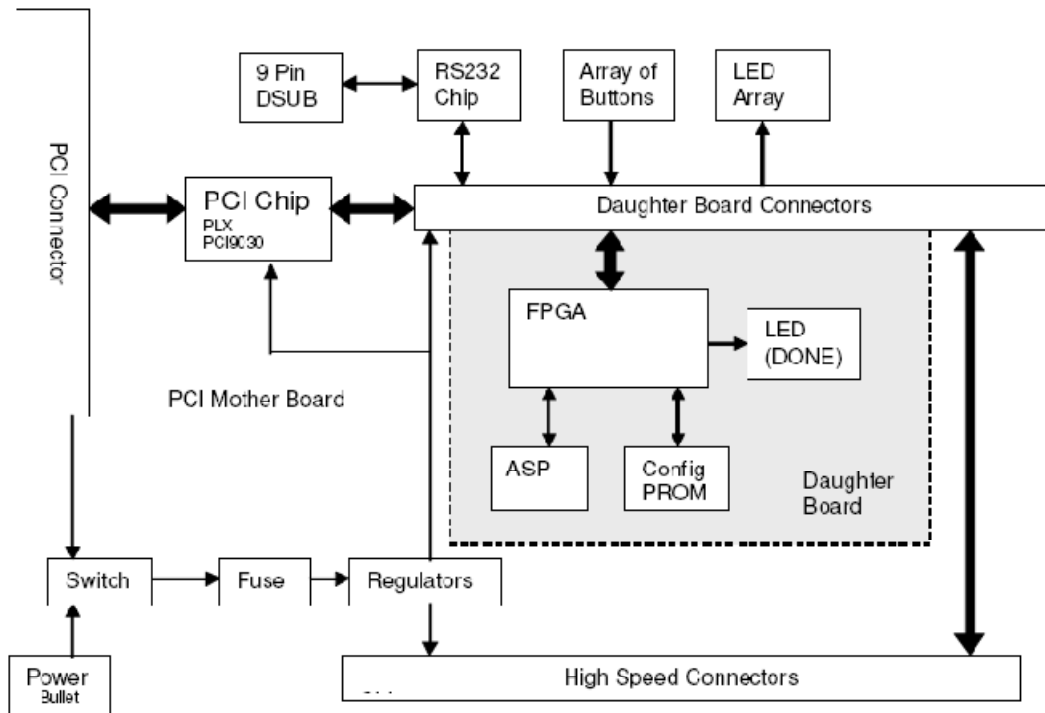


Figure 2 - Block Diagram of PCI/Daughter card